FORM PTO-1390 (REV 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. P101201-00021
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		DATE: June 19, 2001
		U.S. APPLN. NO. (IF KNOWN, SEE 37 C.F.R. 1.5) 09/857184
INTERNATIONAL APPLICATION NO. PCT/JP98/05941	INTERNATIONAL FILING DATE December 25, 1998	PRIORITY DATE CLAIMED None

TITLE OF INVENTION: DIVERSITY RECEIVING APPARATUS THAT PREVENTS JUDGMENT ERRORS DURING DECODING AND A CLOCK GENERATING CIRCUIT FOR A DIVERSITY CIRCUIT THAT PREVENTS JUDGMENT ERRORS DURING DECODING

APPLICANT(S) FOR DO/EO/US: Toshinori IINUMA

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
(THE BASIC FILING FEE IS ATTACHED)

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures [35 U.S.C. 371(f)] at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper demand for International Preliminary Amendment was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed [35 U.S.C. 371(c)(2)]
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☒ A translation of the International Application into English [35 U.S.C. 371(c)(2)].

7. ☐ Amendments to the claims of the International Application under PCT Article 19 [35 U.S.C. 371(c)(3)]
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 [35 U.S.C. 371(c)(3)].

9. ☒ An oath or declaration of the inventor(s) [35 U.S.C. 371(c)(4)].

10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 [35 U.S.C. 371(c)(5)].

Items 11 - 16 below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
CHECK NO. 319546
Drawings (8 sheets)
Notification of Change of Name and Address
International Search Report
Japanese Language Request Form
International Publication No. WO00/39976
Notification of Transmittal of Copies of Translation of the Intl. Prelim. Exam. Rpt. (PCT/IB/338)

JC03 Rec'd PCT/PTO 19 JUN 2001

U.S. APPLN. NO. (IF KNOWN SEE 37 C.F.R. 1.5) 09/857184	INTERNATIONAL APPLICATION NO. PCT/JP98/05941	ATTORNEY DOCKET NO. P101201-00021 DATE: June 19, 2001

17. ☐ The following fees are submitted:

Basic National Fee [37 C.F.R. 1.492(a)(1)-(5)]:	CALCULATIONS	PTO USE ONLY
Search Report has been prepared by the EPO or JPO.....$860.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482).....$690.00 No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO [37 C.F.R. 1.445(a)(2)].....$710.00 Neither international preliminary examination fee (37 C.F.R. 1.482) or international search fee [37 C.F.R. 1.445(a)(2)] paid to USPTO.....$1,000.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(e)].				$	
Claims	Number Filed	Number Extra	Rate		
Total Claims	13 - 20 =	0	X $ 18.00		
Independent Claims	4 - 3 =	1	X $ 80.00	$ 80.00	
Multiple dependent claim(s) (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 940.00	
Reduction by one-half for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 940.00	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 940.00	
Fee for recording the enclosed assignment [37 C.F.R. 1.21(h)]. The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 980.00	
				Amount to be refunded	$
				Charged	$

a. ☒ A check in the amount of $980.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 01-2300 in the amount of $ to cover the above fee. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2300.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive [37 C.F.R. 1.137(a) or (b)] must be filed and granted to restore the application to pending status.

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DESCRIPTION

TITLE OF THE INVENTION

DIVERSITY RECEIVING APPARATUS THAT PREVENTS JUDGEMENT ERRORS DURING DECODING AND A CLOCK GENERATING CIRCUIT FOR A DIVERSITY CIRCUIT THAT PREVENTS JUDGEMENT ERRORS DURING DECODING

TECHNICAL FIELD

The present invention relates to a diversity receiving apparatus for use by a radio communication device and to a clock generating circuit for use by a diversity receiving apparatus.

BACKGROUND ART

Digital radio communication devices conventionally transfer information by modulating a carrier wave using a baseband signal that corresponds to the information to be transmitted.

A variety of digital modulation methods have been used to modulate the carrier wave. With ASK (Amplitude Shift Keying), the amplitude of the carrier wave signal changes according to the baseband signal. With FSK (Frequency Shift Keying), the frequency of the carrier wave is changed. With PSK (Phase Shift Keying), the phase of the carrier wave is changed. With QAM

(Quadrature Amplitude Modulation) the amplitude and phase of the carrier wave are independently changed.

Radio communication devices that receive signals that have been modulated using the digital modulation methods described above demodulate the received signals by performing the opposite of the modulation processing to obtain the original data.

When digital modulation methods are used for mobile communication, it is well known that reception characteristics can be seriously affected by fading, a name given to wild fluctuations in the reception level due to the reflection and scattering of radio waves.

Diversity reception methods are effective in compensating for the decreases in reception level due to fading. Diversity reception methods have the same signal received via a plurality of reception systems and combine a plurality of received signals to produce a high-quality reception signal.

Several diversity reception methods are available. A selection combining method selects the received signal with the highest level out of the signals received by each reception system and demodulates the selected reception signal. An equal-gain combining method combines the reception signals of each reception system at the same level and demodulates the resulting signal. A maximal-ratio combining method gives a

weighting to the reception signal of each reception system in proportion to its relative reception level, combines the weighted reception signals, and demodulates the result.

Of the above methods, the maximal-ratio combining method combines signals after assigning higher weightings to signals with higher reception levels. This means that signals with lower levels of noise are assigned higher weightings, so that reception signals are effectively combined by this method.

The following is a description of a diversity receiving apparatus that uses the maximal-ratio combining method.

Fig. 8 shows the construction of a diversity receiving apparatus that uses the maximal-ratio combining method.

This diversity receiving apparatus is a reception device that receives transmission data which has been modulated using QPSK. The diversity receiving apparatus decodes the transmission data by performing QPSK demodulation and by combining signals that are weighted according to their relative reception levels.

QPSK refers to a transmission method for two-bit (four-value) information. First, two orthogonal carrier waves are separately subjected to phase modulation according to a two-bit baseband signal. The two

modulated signals resulting from the modulation are then added and transmitted. A reception device performs the opposite processing to the QPSK modulation and so obtains two-bit (four-value) information for each symbol.

As shown in Fig. 8, the diversity reception apparatus includes phase demodulating units 329~332, I component ROMs 317~320, Q component ROMs 321~324, an I component adder 325, a Q component adder 326, a judging unit 327, and a clock generating unit 328.

The phase demodulating units 329~332 detect phase differences between the phase of the received reception signal and the phase of the immediately preceding symbol. The phase demodulating units 329~332 output the results as phase data θk (where k=1,2,3,4). Here, the values k=1,2,3,4 respectively correspond to the phase demodulating units 329, 330, 331, and 332.

In detail, the phase demodulating unit 329 includes the input terminal 301, the phase detecting unit 305, the phase delaying unit 309, and the phase adding unit 313. This composes a phase detection-type delay detection device corresponding to the PSK (Phase Shift Keying) modulation method.

The input terminal 301 is a terminal through which a reception signal, which has been digitized by an A/D converter or a limiter, is inputted into the present diversity receiving apparatus.

The phase detecting unit 305 compares the phase of the reception signal inputted via the input terminal 301 with the phase of a local oscillator (not illustrated) and outputs the detected phase value that has been digitized. This means that the phase detecting unit 305 detects only the phase component of the reception signal. Since the amplitude component of the reception signal is not required by the phase detecting unit 305, a linear amplifier is not required.

The phase delaying unit 309 delays the detected phase outputted by the phase detecting unit 305 by the time equivalent to one symbol, and outputs the result as the delayed phase.

The phase adding unit 313 detects the phase difference between the detected phase and the delayed phase and outputs this as the phase data θ1.

The phase demodulating units 330~332 have the same construction as the phase demodulating unit 329 and so output the phase data θ2~θ4.

The I component ROMs 317 ~ 320 and the Q component ROMs 321 ~ 324 respectively correspond to the phase demodulating units 329~332. Using the combining coefficients Rk (k=1,2,3,4) and the phase data θk (k=1,2,3,4), these ROMs output the in-phase components $Rk^2*\cos\theta k$ (k=1,2,3,4) of the reception signals and the quadrature components $Rk^2*\sin\theta k$ (k=1,2,3,4) of the

reception signals that have both been weighted using the combining coefficients Rk.

These combining coefficients Rk are signals showing the signal levels (RSSI: Received Signal Strength Indicator) that have been detected by a high-frequency receiving unit (not illustrated) in each phase demodulating unit 329~332.

The I component ROMs 317~320 store beforehand the input reception signals $Rk^2*\cos\theta k$ (k=1,2,3,4) for the in-phase components for every possible combination of the combining coefficients Rk (k=1,2,3,4) and phase data θk (k=1,2,3,4).

Both the combining coefficients Rk and phase data θk are 8 bits long. The I component ROMs 317~320 store calculation results for all combinations of the 2^8 different values of Rk and the 2^8 different values of θk, which is to say 2^{16} different calculation results. When the combining coefficients Rk and different values of the phase data θk are inputted, the I component ROMs 317~320 output the values of $Rk^2*\cos\theta k$ corresponding to the inputted combination.

In the same way, the Q component ROMs 321~324 store beforehand the input reception signals $Rk^2*\sin\theta k$ (k=1,2,3,4) for the quadrature components for every possible combination of the combining coefficients Rk (k=1,2,3,4) and phase data θk(k=1,2,3,4). When the

combining coefficients Rk and different values of the phase data θk are inputted, the Q component ROMs 321~324 output the values of $Rk^2*\sin\theta k$ corresponding to the inputted combination.

The I component adder 325 combines the weighted in-phase components $Rk^2*\cos\theta k$ (k=1,2,3,4) of the reception signals that have been outputted by the I component ROMs 317~320 and outputs the combined in-phase components of the reception signals.

The Q component adder 326 combines the weighted quadrature components $Rk^2*\sin\theta k$ (k=1,2,3,4) of the reception signals that have been outputted by the Q component ROMs 321~324 and outputs the combined quadrature components of the reception signals.

The clock generating unit 328 extracts symbol sections from the combined in-phase components and quadrature components of the reception signals outputted by the I component adder 325 and the Q component adder 326. Based on the extracted symbol sections, the clock generating unit 328 generates a clock that serves as the standard for the judgement timing of the judging unit 327.

The judging unit 327 outputs two-bit (four value) data by judging whether the combined in-phase components and quadrature components of the reception signals outputted by the I component adder 325 and the Q

component adder 326 are positive or negative. The judging unit 327 performs these judgements in synchronization with the clock generated by the clock generating unit 328.

In this way, a diversity receiving apparatus that uses the conventional maximal-ratio combining method decodes data from a reception signal.

There are cases with conventional diversity receiving apparatuses, however, where the extraction timing of symbol sections significantly deviates within the clock generating unit 328. In such case, the clock generating unit 328 generates a clock with deviated timing. Since the judging unit 327 operates in synchronization with this clock, the judging unit 327 will perform its judgements with a non-optimal judgement timing. This can result in the judging unit 327 making erroneous judgements.

DISCLOSURE OF INVENTION

In view of the stated problems, it is a first object of the present invention to provide a diversity receiving apparatus and a clock generating circuit for a diversity receiving apparatus that prevent deviation in the symbol section extraction by a clock generating unit and so prevent a judging unit from making judgement

errors.

The first object of the present invention can be achieved by a diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal, combines the weighted reception signals, extracts symbol sections in the combined reception signals, and generates a clock for detecting symbols, the diversity receiving apparatus including: a judging unit for judging whether every combining coefficient is below a predetermined threshold; a multiplying unit for uniformly multiplying every combining coefficient when the judging unit judges that every combining coefficient is below the predetermined threshold; and a combining unit for combining the reception signals using the multiplied combining coefficients.

With the stated construction, the combining coefficients are uniformly multiplied if every combining coefficient is below the predetermined threshold. This increases the dynamic range of the combined reception signals. As a result, when the present diversity receiving apparatus extracts the symbol sections based on the combined reception signals, the zero-cross points that mark the extraction timing can be extracted with high precision. This prevents deviation in the symbol

extraction, and so prevents a clock from being generated with deviated timing. This has the effect of reducing the number of judgement errors that occur when judging symbols in synchronization with the generated clock.

Here, the combining coefficients may be one of an received signal strength for each reception system and a parameter showing a reliability of the reception signal obtained by each reception system.

With the stated construction, the diversity receiving apparatus of the present invention can use either a received signal strength or a parameter showing the reliability of a reception signal as a combining coefficient for the reception signal.

Here, the multiplying unit may multiply every combining coefficient by a constant when the judging unit judges that every combining coefficient is below the predetermined threshold.

With the stated construction, the diversity receiving apparatus of the present invention does not need to use a standard multiplier, and instead can multiply the combining coefficients using a multiplier that can only multiply values by a constant. This reduces the hardware scale of the diversity receiving apparatus.

Here, the constant may be related to a result of dividing a maximum value for the combining coefficients

by the threshold.

As a result, the diversity receiving apparatus of the present invention can ensure that the combining coefficients that have been uniformly multiplied by the constant will not exceed the full range for the combining coefficients.

Here, each combining coefficient may be expressed using a predetermined number of bits, the constant being 2^n and the predetermined threshold being found by dividing a maximum value that can be expressed using the predetermined number of bits by 2^n, where $1 \leq n <$ the predetermined number of bits.

With the stated construction, the multiplying unit can be realized by a shifter, thereby simplifying the construction of the diversity receiving apparatus of the present invention.

The stated object can also be achieved by a diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal, combines the weighted reception signals, extracts symbol sections in the combined reception signals, and generates a clock for detecting symbols, the diversity receiving apparatus including: a judging unit for judging whether every combining coefficient is below a predetermined threshold;

a multiplying unit for uniformly multiplying every combining coefficient when the judging unit judges that every combining coefficient is below the predetermined threshold; a combining unit for combining the reception signals using the multiplied combining coefficients; and a generating unit for generating a clock that is synchronized with the reception signals of the reception systems using the reception signals combined by the combining unit.

With the stated construction, the combining coefficients are uniformly multiplied if every combining coefficient is below the predetermined threshold. This increases the dynamic range of the combined reception signals. As a result, when the present diversity receiving apparatus extracts the symbol sections based on the combined reception signals, the zero-cross points that mark the extraction timing can be extracted with high precision. This prevents deviation in the symbol extraction, and so prevents a clock from being generated with deviated timing. This has the effect of reducing the number of judgement errors that occur when judging symbols in synchronization with the generated clock.

The stated object can also be achieved by a diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective

amplitude component of each reception signal, combines the weighted reception signals, and generates a clock for detecting symbols based on the combined reception signals, the diversity receiving apparatus including: a judging unit for judging whether every combining coefficient is below a predetermined threshold; a multiplying unit for doubling every combining coefficient when the judging unit judges that every combining coefficient is below the predetermined threshold; a control unit for repeatedly activating the judging unit and multiplying unit until the judging unit judges that at least one of the combining coefficients is no longer below the predetermined threshold; a combining unit for combining the reception signals using the multiplied combining coefficients when the judging unit judges that at least one of the combining coefficients is no longer below the predetermined threshold; and a generating unit for generating a clock that is synchronized with the reception signals of the plurality of reception systems using the reception signals combined by the combining unit.

With the stated construction, the diversity receiving apparatus of the present invention can achieve the effects described above.

The stated object can also be achieved by a clock generating circuit for use by a diversity receiving

apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal and combines the weighted reception signals, the clock generating circuit including: a judging unit for judging whether every combining coefficient is below a predetermined threshold; a multiplying unit for multiplying every combining coefficient when the judging unit judges that every combining coefficient is below the predetermined threshold; a combining unit for combining the reception signals using the multiplied combining coefficients; and a generating unit for generating a clock that is synchronized with the reception signals of the plurality of reception systems using the reception signals combined by the combining unit.

With the stated construction, the combining coefficients are uniformly multiplied if every combining coefficient is below the predetermined threshold. This increases the dynamic range of the combined reception signals. As a result, when symbol sections are extracted based on the combined reception signals, the zero-cross points that mark the extraction timing can be extracted with high precision, meaning that the present clock generating circuit can generate a clock without deviation.

BRIEF DESCRIPTION OF DRAWINGS

These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings which illustrate a specific embodiment of the invention. In the drawings:

Fig. 1 shows a diversity receiving apparatus for the maximal-ratio combining method according to the first embodiment of the present invention;

Fig. 2 is a block diagram showing the construction of the converting unit 314 in more detail;

Figs. 3A and 3B are graphs showing values of the reception level Ck (k=1,2,3,4) that are inputted into the converting unit 314 before and after conversion;

Fig. 4 is a block diagram showing the construction of the judging unit 202 in more detail;

Fig. 5 is a block diagram showing an example construction of the multipliers 203~206 in detail;

Fig. 6 is a flowchart showing the processing of the converting unit 314 in the second embodiment;

Fig. 7 shows the eye pattern of the phase data in QPSK (where the multiple sets of phase data have been plotted in synchronization for each modulation phase); and

Fig. 8 shows a conventional diversity receiving

apparatus for the maximal-ratio combining method.

BEST MODE FOR CARRYING OUT THE INVENTION

First Embodiment

Fig. 1 shows a diversity receiving apparatus for the maximal-ratio combining method according to the first embodiment of the present invention.

The present diversity receiving apparatus gives the in-phase components and quadrature components of the reception signal received by the four reception systems a weighting (through multiplication by a combining coefficient) based on the reception level (RSSI: Received Signal Strength Indicator) of each reception signal. The diversity receiving apparatus then combines the weighted reception signals. After this, the diversity receiving apparatus judges the sign ("plus" or "minus") of the combined in-phase components of the reception signals and the combined quadrature components of the reception signals to obtain two-bit (four value) decoded data that it outputs. When giving a weighting based on a reception level to the in-phase components and the quadrature components of the reception signals, the present diversity receiving apparatus uniformly amplifies each reception level before giving the weighting if every reception level is below a predetermined threshold.

When performing the sign judgement, the present diversity receiving apparatus extracts symbol sections based on the combined in-phase components and quadrature components of the reception signals and generates a clock that sets the judgement timing according to the extracted symbol sections.

To operate as described above, the present diversity receiving apparatus includes a converting unit 314, phase detection units 329~332, I component ROMs 317~320, Q component ROMs 321~324, an I component adder 325, a Q component adder 326, a judging unit 327, and a clock generating unit 328.

The converting unit 314 receives an input of the reception levels Ck (k=1,2,3,4) corresponding to the phase detection units 329~332 and judges whether every reception level Ck (k=1,2,3,4) is below a predetermined threshold (or in other words, whether there is at least one reception level that exceeds the predetermined threshold).

If the result of this judgement is that all reception levels Ck (k=1,2,3,4) are below the predetermined threshold, the converting unit 314 uniformly multiplies the reception levels Ck to produce the combining coefficients Tk that the converting unit 314 then outputs.

Conversely, when the converting unit 314 judges

that at least one reception level exceeds the predetermined level, the converting unit 314 outputs the reception levels Ck (k=1,2,3,4) without amendment as the combining coefficients Tk (k=1,2,3,4).

The reception levels inputted into the converting unit 314 are signals that have been detected by high-frequency receiving units (not illustrated) in the phase demodulating units 329~332, and as one example are eight-bit digital data. The uniform multiplication described here refers to the multiplication of the four reception levels by a predetermined multiplier so that the reception levels are increased with the ratio between their values being maintained.

The phase demodulating units 329~332 detect the phase difference between the phase of each received reception signal and the phase of the immediately preceding symbol section in the signal, and output the results as the phase data θk(k=1,2,3,4). Here, the values k=1,2,3,4 respectively correspond to the phase demodulating units 329, 330, 331, and 332.

In detail, the phase demodulating unit 329 includes an input terminal 301, a phase detecting unit 305, a phase delaying unit 309, and a phase adding unit 313. This composes a phase-detection type delay detection device corresponding to the PSK (Phase Shift Keying) modulation method.

The input terminal 301 is a terminal through which a reception signal, which has been digitized by an A/D converter or a limiter, is inputted into the present diversity receiving apparatus.

The phase detecting unit 305 compares the phase of the reception signal inputted via the input terminal 301 with the phase of a local oscillator (not illustrated) and outputs the detected phase value that has been digitized. This means that the phase detecting unit 305 detects only the phase component of the reception signal. Since the amplitude component of the reception signal is not required by the phase detecting unit 305, a linear amplifier is not required.

The phase delaying unit 309 delays the detected phase outputted by the phase detecting unit 305 by the time equivalent to one symbol, and outputs the result as the delayed phase.

The phase adding unit 313 detects the phase difference between the detected phase and the delayed phase and outputs this as the phase data θ1.

The phase demodulating units 330~332 have the same construction as the phase demodulating unit 329 and so output the phase data θ2~θ4.

The I component ROMs 317 ~ 320 and the Q component ROMs 321 ~ 324 respectively correspond to the phase demodulating units 329~332. Using the combining

coefficients Tk (k=1,2,3,4) and the phase data θk (k=1,2,3,4), these ROMs output the in-phase components $Tk^2*\cos\theta k$ (k=1,2,3,4) of the reception signals and the quadrature components $Tk^2*\sin\theta k$ (k=1,2,3,4) of the reception signals that have both been weighted using the combining coefficients Tk.

The I component ROMs 317~320 store beforehand the in-phase components $Tk^2*\cos\theta k$ (k=1,2,3,4) of the reception signals for every possible combination of the combining coefficients Tk (k=1,2,3,4) and phase data θk (k=1,2,3,4).

Both the combining coefficients Tk and phase data θk are 8 bits long. The I component ROMs 317~320 store calculation results for all combinations of the 2^8 different values of Tk and the 2^8 different values of θk, which is to say 2^{16} different calculation results. When the combining coefficients Tk and different values of the phase data θk are inputted, the I component ROMs 317~320 output the values of $Tk^2*\cos\theta k$ corresponding to the inputted combination.

In the same way, the Q component ROMs 321~324 store beforehand the quadrature components $Tk^2*\sin\theta k$ (k=1,2,3,4) of the reception signals for every possible combination of the combining coefficients Tk (k=1,2,3,4) and phase data θk(k=1,2,3,4). Both the combining coefficients Tk and phase data θk are 8 bits long so that

the Q component ROMs 321~324 store calculation results for all combinations of the 2^8 different values of Tk and the 2^8 different values of θk, which is to say 2^{16} different calculation results. When the combining coefficients Tk and the different values of the phase data θk are inputted, the Q component ROMs 321~324 output the values of $Tk^2*\sin\theta k$ corresponding to the inputted combination.

The I component adder 325 combines the weighted in-phase components $Tk^2*\cos\theta k$ (k=1,2,3,4) that have been outputted by the I component ROMs 317~320 and outputs the combined in-phase components of the reception signals.

The Q component adder 326 combines the weighted quadrature components $Tk^2*\sin\theta k$ (k=1,2,3,4) that have been outputted by the Q component ROMs 321~324 and outputs the combined quadrature components of the reception signals.

The clock generating unit 328 includes the symbol section detecting unit 333 and the PLL (Phase Locked Loop) unit 334. With this construction, the clock generating unit 328 generates a clock according to the combined in-phase components and quadrature components of the reception signals outputted by the I component adder 325 and the Q component adder 326. This clock is used as the standard for the judgement timing of the judging unit 327.

In more detail, the symbol section detecting unit 333 detects symbol sections based on the combined in-phase components and the quadrature components outputted by the I component adder 325 and the Q component adder 326. The symbol section detecting unit 333 detects the symbol sections by detecting the zero cross points of the combined in-phase components and quadrature components of the reception signals.

The PLL unit 330 generates a clock that is used as the standard for the judgement timing of the judging unit 327 according to the symbol sections detected by the symbol section detecting unit 333.

In this way, the clock generating unit 328 generates a clock according to a self-timing method that generates the clock in synchronization with the reception signals, based on the combined in-phase components and quadrature components of the reception signals.

The judging unit 327 outputs two-bit (four value) data by judging whether the combined in-phase components and quadrature components of the reception signals outputted by the I component adder 325 and the Q component adder 326 are positive or negative. The judging unit 327 performs these judgements in synchronization with the clock generated by the clock generating unit 328.

In the judging unit 327, deviations (clock phase

errors) that can cause judgement errors are present in the clock inputted by the clock generating unit 328. If there are deviations in the clock inputted into the judging unit 327, the judging unit 327 can end up performing the judgement with a timing that deviates somewhat from the ideal timing. This increases the probability of erroneous judgements being made.

To prevent erroneous judgements from being made, the clock generating unit 328 needs to generate the clock with high precision. To enable the clock generating unit 328 to do this, the symbol section detecting unit 333 needs to correctly detect the symbol sections in the combined reception signals. Here, the higher the dynamic range of the inputted combined in-phase components and quadrature components of the reception signals, the higher the accuracy with which the symbol section detecting unit 333 can detect the zero cross points in the combined reception signals when detecting the symbol sections.

Based on the above, the diversity receiving apparatus of the present invention uniformly multiplies the reception levels if every reception level is below a predetermined threshold. Since these multiplied reception levels are used as the combining coefficients, the combined in-phase components and the quadrature components of the reception signals produced by the

combining will have a high dynamic range.

Fig. 2 is a block diagram showing the construction of the converting unit 314 in more detail.

The converting unit 314 includes the judging unit 202 and the multipliers 203~206. As shown by the examples in Figs. 3A and 3B, if every reception level Ck (k=1,2,3,4) is below the threshold, the converting unit 314 multiplies each reception level uniformly by the constant N.

Here, it is preferable for the threshold to be a value in a range that is 1/8 ~ 1/4 of the full range of the reception level Ck. The constant N is a value that is one or greater. This value may be set at a value that is equal to or smaller than the inverse of the threshold. In the present embodiment, the constant N is four. The reason the threshold and the constant N may be in an inverse relationship is that this ensures that a value that is N times the reception level Ck will not exceed the full range of the reception level Ck.

On receiving the four reception levels Ck, the judging unit 202 judges whether all of these reception levels Ck are below the threshold. If so, the judging unit 202 outputs the judgement signal 207 that gives notice of this.

When the judgement signal 207 has been inputted from the judging unit 202, the multipliers 203~206

multiply the reception levels Ck by the constant N and output the results as the combining coefficients Tk. This means that Tk=Ck*N (k=1,2,3,4). When the judgement signal is not inputted from the judging unit 202, the multipliers 203~206 respectively output the reception level Ck as the combining coefficient Ck.

Fig. 4 is a block diagram showing the construction of the judging unit 202 in more detail.

The judging unit 202 includes the comparators 401~404 and the AND circuit 405.

The comparators 401~404 respectively compare the magnitudes of the reception levels Ck (k=1,2,3,4) with the threshold. When the threshold is greater than a respective reception level Ck, the comparators each output a signal Sk (k=1,2,3,4) to the AND circuit 405.

The AND circuit 405 outputs the judgement signal 207 only when all four signals Sk (k=1,2,3,4) have been inputted, which is to say, only if every reception level Ck is below the threshold.

Fig. 5 is a block diagram showing an example construction of the multipliers 203~206 in detail.

The multipliers 203~206 include the selectors 501~508 and are configured so as to produce a product of a constant and an inputted eight-bit reception level Ck.

The selectors 501~508 output the signals inputted from the eight input terminals A to the output terminals

X when the judgement signal 207 is not inputted from the judging unit 202, and output the signals inputted from the eight input terminals B to the output terminals X when the judgement signal 207 is inputted.

An eight bit signal representing the reception level Ck is inputted into the input terminals A of the selectors 501~508 in parallel. The most significant bit (MSB) of the reception level Ck is inputted into the selector 501 and the least significant bit (LSB) is inputted into the selector 508. A bit value at two bit positions lower in the eight-bit reception signal Ck is inputted into the B input terminals of the selectors 501~506, while the value "0" is inputted into the B terminals of the selectors 507 and 508. As a result, the multipliers 203 ~ 206 output Tk=Ck when the judgement signal 207 is not inputted, and output Tk=Ck*4 when the judgement signal 207 is inputted.

The following is an explanation of the operation of a diversity receiving apparatus of the first embodiment of the present invention whose construction has been described above.

Fig. 3A is a graph showing values of the reception level Ck (k=1,2,3,4) that are inputted into the converting unit 314. In Fig. 3A, the vertical axis shows the full range ("MAX") for the combining coefficients with the threshold as 1/4 of the full range. Each

reception level Ck in Fig. 3A is below the threshold value.

When the reception levels Ck shown in Fig. 3A are inputted into the converting unit 314, the judging unit 202 compares the magnitudes of the reception levels Ck with the threshold. Since this comparison finds that every reception level Ck is below the threshold, the judging unit 202 outputs the judgement signal 207 to the multipliers 203~206.

When the judgement signal 207 has been inputted from the judging unit 202, the multipliers 203~206 shift the bit values in the reception level Ck upwards by two bits.

Fig. 3B is a graph showing the combining coefficients Tk that are outputted by the converting unit 314 when the reception levels Ck shown in Fig. 3A are inputted into the converting unit 314.

Meanwhile, when a reception signal is inputted, the phase demodulating units 329~332 detect the phase component having removed the amplitude component of the reception signals. The phase demodulating units 329~332 output phase data θk (k=1,2,3,4) obtained as the phase difference between the detected phase component and the delayed phase.

The I component ROMs 317~320 and the Q component ROMs 321~324 receive an input of the combining

coefficients Tk and the phase data θk and output $Tk^2*\cos\theta k$ and $Tk^2*\sin\theta k$.

The I component adder 325 and the Q component adder 326 respectively combine the different values of $Tk^2*\cos\theta k$ and $Tk^2*\sin\theta k$ and output the results as the combined in-phase components and the quadrature components of the reception signals to the clock generating unit 328 and the judging unit 327.

Here, the lower the value of Tk, the lower the dynamic range of the combinedin-phase components and quadrature components of the reception signals. As mentioned earlier, a low dynamic range adversely affects the detection of the symbol sections by the clock generating unit 328. Accordingly, the present diversity receiving apparatus has the converting unit 314 multiply the combining coefficients Tk, so that a wide dynamic range is maintained for the combined in-phase components and quadrature components $Tk^2*\cos\theta k$ and $Tk^2*\sin\theta k$. This avoids the adverse effects described earlier.

The judging unit 327 judges whether the combined in-phase components and quadrature components of the reception signals are positive or negative based on the clock that is highly precisely generated by the clock generating unit 328. The judging unit 327 outputs the result of its judgement as the decoded data.

Second Embodiment

The overall construction of the diversity receiving apparatus in the second embodiment of the present invention is the same as that shown in Fig. 1, though the converting unit 314 has a different internal configuration. This difference is that the converting unit 314 is composed of a microprocessor or a DSP (Digital Signal Processor).

Fig. 6 is a flowchart showing the processing of the converting unit 314 in the second embodiment.

The converting unit 314 stores the largest signal value out of the four inputted reception levels Ck (k=1,2,3,4) in the register A (Step 601). The converting unit 314 then substitutes the initial value 0 into the variable N (Step 602).

Next, the converting unit 314 compares the value in the register A with a threshold (here set at half the full range). When the value in the register A is larger than the threshold (Step 603:Yes), the converting unit 314 proceeds to Step 606 and then terminates its processing. When the value in register A is equal to or below the threshold (Step 603:No), the converting unit 314 increments the value of the variable N by one (Step 604), stores a value that is double the value of register A into register A, and then returns to Step 603.

In this way, the processing in Steps 603~605 is

repeated until the value in the register A exceeds the threshold. When the value in the register A exceeds the threshold (Step 603:Yes), the converting unit 314 finds the value $Ck*2^N$ for each reception level and sets the resulting values as the combining coefficients Tk (k=1,2,3,4).

In the first and second embodiments, the reception level Ck is described as being a reception level signal (RSSI), although a parameter (alienation value) that shows the reliability of the received information may be used in place of the reception level signal.

Fig. 7 shows the eye pattern of the phase data in QPSK (where the multiple sets of phase data have been plotted in synchronization for each modulation phase). The alienation values L1 and L2 are likelihood values for the ideal judging points for judging the phase data. The larger the alienation values, the closer the judging point to the ideal, which is to say the lower the proportion of noise in the reception signal.

In this way, the converting unit 314 of the diversity receiving apparatus of the present invention uniformly multiplies the value of each reception level on judging that the value of each reception level Ck is below a threshold and outputs the resulting values as the combining coefficients Tk. As a result, a high dynamic

range can be maintained for the combined in-phase components and quadrature components of the reception signals that are outputted to the clock generating unit 328 via the I component ROMs 317~320, the Q component ROMs 321~324, the I component adder 325, and the Q component adder 326.

The symbol section detecting unit 333 can detect the symbol sections with high precision based on the combined in-phase components and quadrature components of the reception signals whose dynamic range has been expanded. The PLL unit 334 generates a highly precise clock, which is to say a clock that is precisely synchronized with the original reception signals, based on the detected symbol sections. This means that the judging unit 327 can perform its judgement with a judgement timing that is closer to the ideal judgement timing. This reduces the probability of judgement errors being made.

INDUSTRIAL APPLICABILITY

The diversity receiving apparatus of the present invention can prevent deviations in the generation of a clock by the clock generating unit when the reception levels are low and prevent the judging unit from making judgement errors. This is of particular use to mobile communication devices where deterioration in the

reception level is often caused by fading and other factors.

CLAIMS

1. A diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal, combines the weighted reception signals, extracts symbol sections in the combined reception signals, and generates a clock for detecting symbols,

the diversity receiving apparatus comprising:

judging means for judging whether every combining coefficient is below a predetermined threshold;

multiplying means for uniformly multiplying every combining coefficient when the judging means judges that every combining coefficient is below the predetermined threshold; and

combining means for combining the reception signals using the multiplied combining coefficients.

2. The diversity receiving apparatus of Claim 1,

wherein the combining coefficients are one of an received signal strength for each reception system and a parameter showing a reliability of the reception signal obtained by each reception system.

3. The diversity receiving apparatus of Claim 2,

wherein the multiplying means multiplies every combining coefficient by a constant when the judging means judges that every combining coefficient is below the predetermined threshold.

4. The diversity receiving apparatus of Claim 3,

wherein the constant is related to a result of dividing a maximum value for the combining coefficients by the threshold.

5. The diversity receiving apparatus of Claim 4,

wherein each combining coefficient is expressed using a predetermined number of bits,

the constant being 2^n and the predetermined threshold being found by dividing a maximum value that can be expressed using the predetermined number of bits by 2^n, where $1 \leq n <$ the predetermined number of bits.

6. A diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal, combines the weighted reception signals, extracts symbol sections in the combined reception signals, and generates a clock for detecting symbols,

the diversity receiving apparatus comprising:

judging means for judging whether every combining coefficient is below a predetermined threshold;

multiplying means for uniformly multiplying every combining coefficient when the judging means judges that every combining coefficient is below the predetermined threshold;

combining means for combining the reception signals using the multiplied combining coefficients; and

generating means for generating a clock that is synchronized with the reception signals of the reception systems using the reception signals combined by the combining means.

7. The diversity receiving apparatus of Claim 6,

wherein the combining coefficients are one of an received signal strength for each reception system and a parameter showing a reliability of the reception signal obtained by each reception system.

8. The diversity receiving apparatus of Claim 7,

wherein the multiplying means multiplies every combining coefficient by a constant when the judging means judges that every combining coefficient is below the predetermined threshold.

9. The diversity receiving apparatus of Claim 8,

wherein the constant is related to a result of dividing a maximum value for the combining coefficients by the threshold.

10. The diversity receiving apparatus of Claim 9,

wherein each combining coefficient is expressed using a predetermined number of bits,

the constant being 2^n and the predetermined threshold being found by dividing a maximum value that can be expressed using the predetermined number of bits by 2^n, where $1 \leq n <$ the predetermined number of bits.

11. A diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal, combines the weighted reception signals, and generates a clock for detecting symbols based on the combined reception signals,

the diversity receiving apparatus comprising:

judging means for judging whether every combining coefficient is below a predetermined threshold;

multiplying means for doubling every combining coefficient when the judging means judges that every combining coefficient is below the predetermined threshold;

control means for repeatedly activating the judging means and multiplying means until the judging means judges that at least one of the combining coefficients is no longer below the predetermined threshold;

combining means for combining the reception signals using the multiplied combining coefficients when the judging means judges that at least one of the combining coefficients is no longer below the predetermined threshold; and

generating means for generating a clock that is synchronized with the reception signals of the plurality of reception systems using the reception signals combined by the combining means.

12. The diversity receiving apparatus of Claim 11,

wherein the combining coefficients are one of an received signal strength for each reception system and a parameter showing a reliability of the reception signal obtained by each reception system.

13. A clock generating circuit for use by a diversity receiving apparatus that separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal and combines the

weighted reception signals,

the clock generating circuit comprising:

judging means for judging whether every combining coefficient is below a predetermined threshold;

multiplying means for multiplying every combining coefficient when the judging means judges that every combining coefficient is below the predetermined threshold;

combining means for combining the reception signals using the multiplied combining coefficients; and

generating means for generating a clock that is synchronized with the reception signals of the plurality of reception systems using the reception signals combined by the combining means.

ABSTRACT

A diversity receiving apparatus separately weights reception signals of a plurality of reception systems using combining coefficients based on a respective amplitude component of each reception signal and combines the weighted reception signals. The diversity receiving apparatus extracts symbol sections in the combined reception signals, and generates a clock for detecting symbols. The diversity receiving apparatus includes a converting unit 314 for uniformly multiplying the combining coefficients if every combining coefficient is below a predetermined threshold and I component ROMs, Q component ROMs, an I component adder 325 and a Q component adder 326 that combine the reception signals using the multiplied combining coefficients.

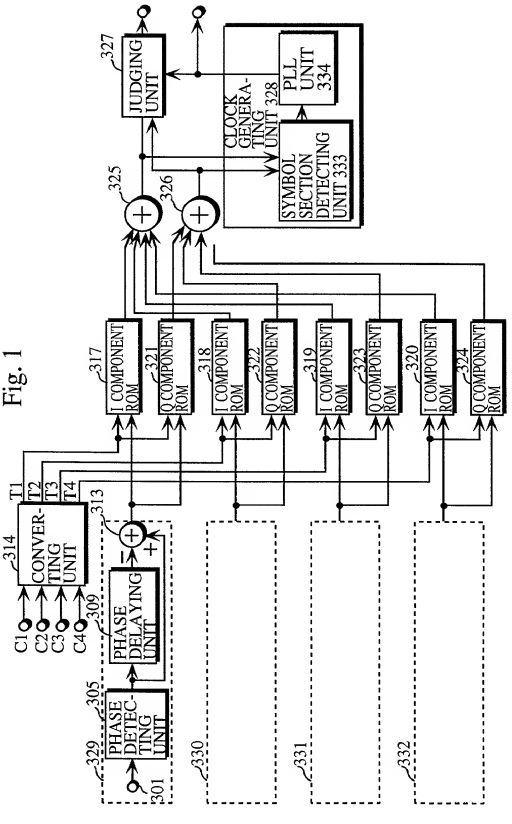

C1
C2
C3
C4
309
314
CONVERTING UNIT
T1
T2
T3
T4
313
PHASE DELAYING UNIT
305
PHASE DETECTING UNIT
301
329
330
331
332
317
I COMPONENT ROM
321
Q COMPONENT ROM
318
I COMPONENT ROM
322
Q COMPONENT ROM
319
I COMPONENT ROM
323
Q COMPONENT ROM
320
I COMPONENT ROM
324
Q COMPONENT ROM
325
326
327
JUDGING UNIT
CLOCK GENERATING UNIT 328
SYMBOL SECTION DETECTING UNIT 333
PLL UNIT 334

Fig. 1

Fig. 2

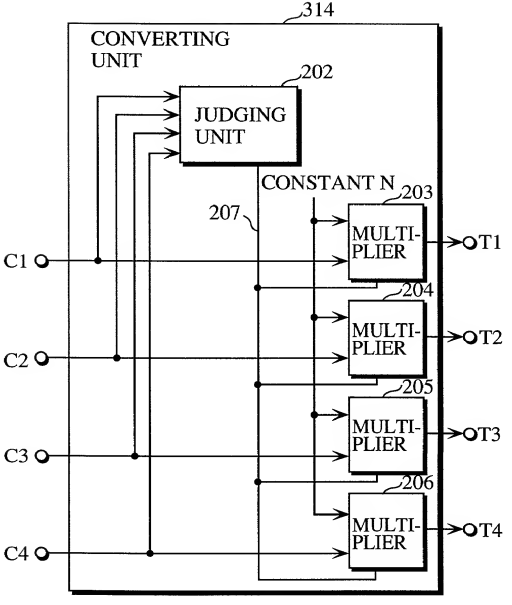

314
CONVERTING UNIT
202
JUDGING UNIT
CONSTANT N
207
203
MULTI-PLIER
204
MULTI-PLIER
205
MULTI-PLIER
206
MULTI-PLIER
C1
C2
C3
C4
T1
T2
T3
T4

Fig. 3A
MAX
THRESHOLD
0
C1
C2
C3
C4
QUADRUPLED
Fig. 3B
MAX
THRESHOLD
0
T1
T2
T3
T4

Fig. 4

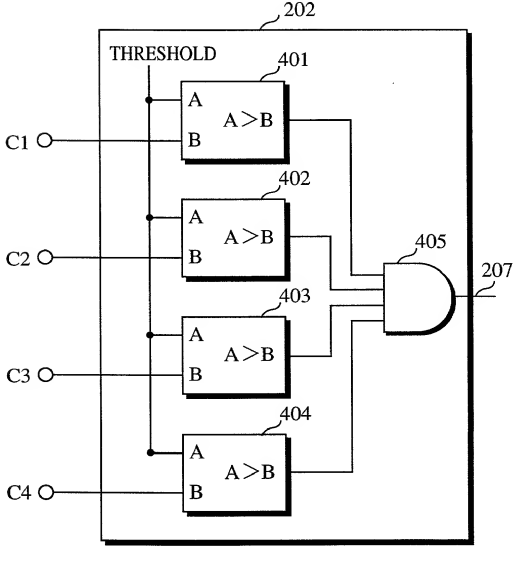

202
THRESHOLD
401
A
B
A>B
C1
402
A
B
A>B
C2
405
207
403
A
B
A>B
C3
404
A
B
A>B
C4

Fig. 5

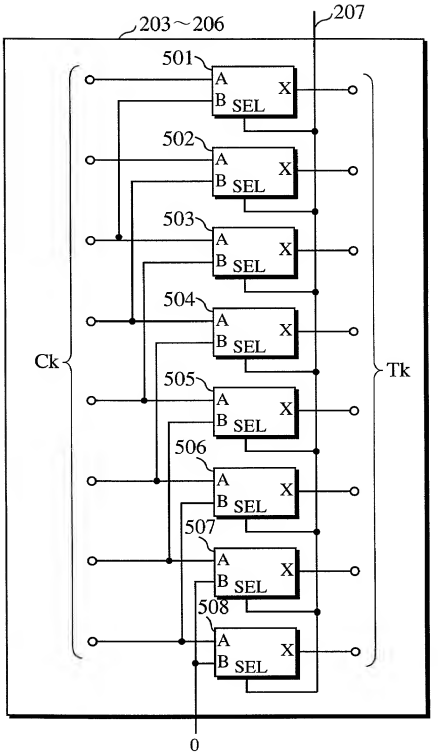


Fig. 6

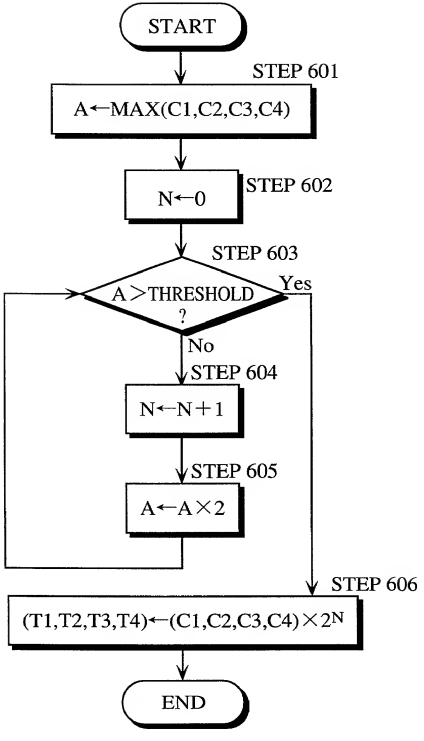

START
STEP 601
A←MAX(C1,C2,C3,C4)
N←0
STEP 602
STEP 603
A＞THRESHOLD ?
Yes
No
STEP 604
N←N＋1
STEP 605
A←A×2
STEP 606
(T1,T2,T3,T4)←(C1,C2,C3,C4)×2N
END

Fig. 7

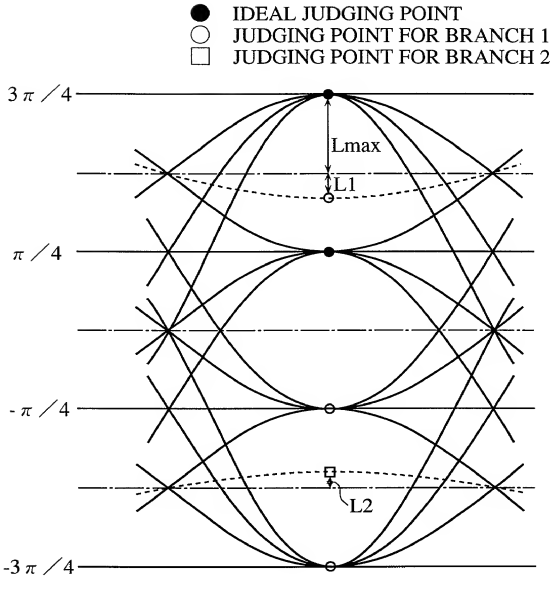
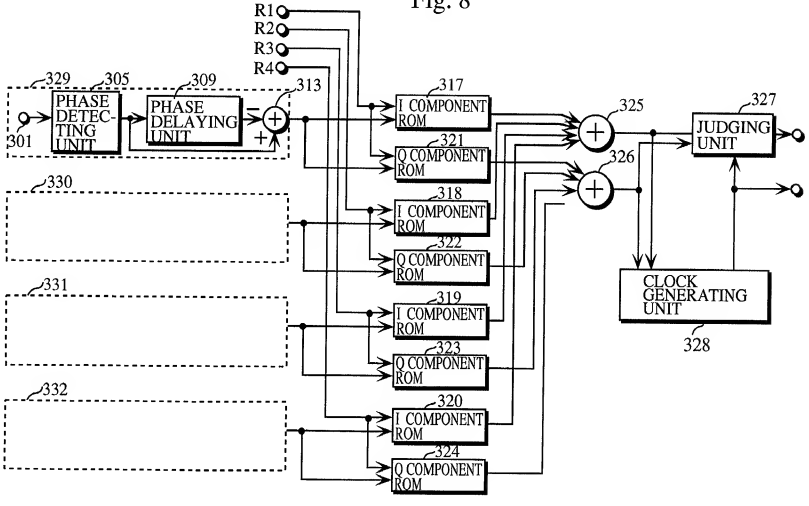

IDEAL JUDGING POINT
JUDGING POINT FOR BRANCH 1
JUDGING POINT FOR BRANCH 2
3 π ／4
π ／4
- π ／4
-3 π ／4
Lmax
L1
L2

Fig. 8



N, M, M & O Docket No. _____ NIKAIDO, MARMELSTEIN, MURRAY & ORAM LLP

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
(Insert Title) DIVERSITY RECEIVING APPARATUS THAT PREVENTS JUDGMENT ERRORS DURING DECODING AND A CLOCK GENERATING CIRCUIT FOR A DIVERSITY
the specification of which is attached hereto unless the following box is checked CIRCUIT THAT PREVENTS JUDGEMENT ERRORS DURING DECODING
☐ was filed on 25/12/98 as PCT International Application
Number PCT/JP98/05941 and was amended on _____
and/or was filed on _____ as United States Application
Number _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. §1.56.
I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International Application having a filing date before that of the application(s) for which priority is claimed:

(List prior foreign applications. See note A on back of this page)	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
	(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
				☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

(See Note B on back of this page) ☐ See attached list for additional prior foreign or provisional applications.

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) or §365(c) of any PCT International application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) (U.S. or PCT) in the manner provided by the first paragraph of 35, U.S.C. §112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(List prior U.S. Applications or PCT International applications designating the U.S.)	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See Note C on back of this page) 1-50

Full name of sole or first inventor Toshinori IINUMA
Inventor's signature Toshinori Iinuma 04/06/01 Date
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Citizenship Japan
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Rev. #12 4/6/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

IINUMA

Serial Number: New Application

Filed: June 19, 2001

For: DIVERSITY RECEIVING APPARATUS THAT PREVENTS JUDGMENT ERRORS DURING DECODING AND A CLOCK GENERATING CIRCUIT FOR A DIVERSITY CIRCUIT THAT PREVENTS JUDGMENT ERRORS DURING DECODING

NOTIFICATION OF CHANGE OF NAME AND ADDRESS

Commissioner for Patents
Washington, D.C. 20231

June 19, 2001

Sir:

Kindly change the correspondence name and address for the above-identified application to the following:

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Should any fees be due with respect to this paper, please charge Counsel's

Deposit Account No. 01-2300.

Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN

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